(assuming right-heavy C & $u \notin \mathcal{F}_m$)

- Case $u = u_1 \times u_2$ with $\deg u_2 \geq m$:

$$[u] = [u_1] \cdot [u_2]$$

$$= [u_1] \cdot \sum_{w \in \mathcal{F}_m} [u_2 : w] \cdot [w]$$

$$= \sum_{w \in \mathcal{F}_m} [u_1 \cdot u_2 : w] \cdot [w] \,,$$

& $[u : v] = [u_1] \cdot [u_2 : v]$

$$= \sum_{w \in \mathcal{F}_m} [u_1] \cdot [u_2 : w] \cdot [w : v]$$

$$= \sum_{w \in \mathcal{F}_m} [u_1 \cdot u_2 : w] \cdot [w : v] \,.$$

□

- Now we are ready to write the depth reduced circuit.

We will take a top-down approach, due to Allender, Jiao, Mahajan, Vinay (1998).

- We shall recursively compute $[u]$, $[u : v]$ from nodes in C of a lower degree.

• Let $\mathcal{F}(u) := \mathcal{F}_m$ for $m := \deg(u)/2 > 1$.

Now, $[u] = \sum_{w \in \mathcal{F}(u)} [u:w] \cdot [w]$

$= \sum_{w \in \mathcal{F}(u)} [u:w] \cdot [w_L] \cdot [w_R]$.

⇒ $[u]$ is an addition gate with fanin < 2, the input mult. gates have fanin ≤ 3. The latter have inputs of deg $\leq \deg(u)/2$.

• Let $\mathcal{F}(u,v) := \mathcal{F}_m$ for $m := \deg(uv)/2 > 1$.

Now, $[u:v] = \sum_{w \in \mathcal{F}(u,v)} [u:w] \cdot [w:v]$

$= \sum_{w \in \mathcal{F}(u,v)} [u:w] \cdot [w_L] \cdot [w_R:v]$.

• Here, $\deg(w_L)$ could be larger than $\max\{1, \deg[u:v]/2\}$. So, we apply the frontier expansion once again.

$= \sum_{\substack{w \in \mathcal{F}(u,v) \\ p \in \mathcal{F}(w_L)}} [u:w] \cdot [w_L:p] \cdot [p_L] \cdot [p_R] \cdot [w_R:v]$

- $\deg [u:w] \leq \deg u - \deg(uv)/2 \leq \frac{\deg[u:v]}{2}$.

- $\deg [w_R:v] \leq \deg(uv)/2 - \deg v \leq$ " .

▷ If $[u:v] \neq 0$ then $\deg [u:w]\cdot[w:v] \leq \deg [u:v]$.

Pf: • Since $[u:v] \neq 0$, we have
$\deg[u:v] = \deg[u] - \deg[v]$.

• We know, $\deg [u:w]\cdot[w:v]$
$\leq \deg[u] - \deg[w] + \deg[w] - \deg[v]$
$= \deg [u:v]$. □

$\Rightarrow \deg [u:w]\cdot[w_L]\cdot[w_R:v] \leq \deg[u:v]$

• So, assuming that w contributes a nonzero summand in expansion, we deduce $\deg[w_L] \leq \deg[u:v]$.

• Finally, $\deg[w_L:p]$, $\deg[p_L]$, $\deg[p_R]$ are all at most $\deg[w_L]/2 \leq \frac{1}{2}\cdot\deg[u:v]$.

$\Rightarrow$ $[u:v]$ is an addition gate with fanin $< s^2$, the input mult. gates have fanin ≤ 5. The latter have inputs of deg $\leq$ deg $[u:v]/2$.

- Eventually, we reach a case where deg $[u]$ or deg $[u:v]$ is at most 2.
  These we can explicitly compute in depth ≤ 2.

- Since each application of frontier expansion halves the degree (of the inputs), we get $O(\lg d)$-depth.
  It can be shown that the size of C' is poly$(s.n.\lg d)$. [Exercise]

- Also, C' has alternating layers of addn, mult gates & the fanin of the latter is bounded (by 5)!

□

Reduction to bare minimum depth

- By the efficient $O(\log d)$-depth reduction we know that: to prove hardness results for a degree d polynomial f it suffices to study $O(\log d)$-depth.

- Now we will reduce this, further, to depth-4.

Theorem [Agrawal-Vinay '08, Koiran '12, Tavenas '15]: Let f be a degree d polynomial computed by a size s circuit. Then, for all $t \in [d]$, f has a homogeneous $\Sigma\Pi^{O(d/t)}\Sigma\Pi^{t}$ circuit of top fanin $s^{O(d/t)}$ & size $s^{O(t+d/t)}$.

[$\Sigma^k\Pi^{d'}\Sigma\Pi^t$ circuit looks like $\sum_{i=1}^{k}\prod_{j=1}^{d'} f_{ij}$ where k is the top fanin & the bottom fanin t bounds the degree of f_{ij}'s.]

[To optimize the size one could take $t=\sqrt{d}$, giving $k \approx \text{size} \approx s^{O(\sqrt{d})}$ which is nontrivial!]