CS330: Operating Systems

Shared address space and concurrency

Recap: Threads

- Threads share the address space
	- Low context switch overheads
	- Global variables can be accessed from thread functions
	- Dynamically allocated memory can be passed as thread arguments
- Sharing data is convenient to design parallel computation
- Pthread API for multi-threaded programming

Threads sharing the address space

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	- Global variables can be accessed from thread functions
- μ - Everything seems to be fine, what is the issue?
- Sharing data is convenient to design parallel computation parallel computation parallel computation parallel computation of the sharing computation of the sharing computation of the sharing computation of the sharing com - How does OS fit into this discussion?
	- Data parallel processing: Data is partitioned into disjoint sets and assigned to different threads
	- Task parallel processing: Each thread performs a different computation on the same data

```
static int counter = o;
void *thfunc(void *)
{
  int ctr = 0;
  for(ctr=0; ctr<100000; ++ctr) counter++;
}
```
- If this function is executed by two threads, what will be the value of counter when two threads complete?

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- Non-deterministic output
- Why?

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 $\left\{ \right.$

counter++ in assembly mov (counter), R1 $Add 1, R1$ Mov R₁, (counter)

Even on a single processor system, scheduling of threads between the above instructions can be problematic!

- T₁: mov (counter), R₁ // R₁ = \circ $Ti: Add 1, R1$ $\{switch-out, R1=1\text{ saved in PCB}\}$
- Assume that T1 is executing the first iteration
- On context switch, value of R1 is saved onto the PCB
- Thread T2 is scheduled and starts executing the loop

- T₁: mov (counter), R_1 // $R_1 = o$ $Ti: Add 1, R1$
- $\{switch-out, R1=1\text{ saved in }PCB\}$
- T2: mov (counter), R1 $//$ R₁ = \circ
- $T2: Add 1, R1$ // $R1 = 1$

T2 mov R1, (counter) // counter = 1 $\{switch-out, T1 scheduled, R1 = 1\}$

- T2 executes all the instructions for one iteration of the loop, saves 1 to counter (in memory) and then, scheduled out
- T1 is switched-in, R1 value (=1) loaded from the PCB

- T₁: mov (counter), R₁ // R₁ = \circ $Ti: Add 1, R1$ $\{switch-out, R1=1\text{ saved in }PCB\}$ T2: mov (counter), R1 $//$ R₁ = \circ
- $T2: Add 1, R1$ // $R1 = 1$
- T2 mov R1, (counter) // counter $= 1$
- $\{switch-out, T1 scheduled, R1 = 1\}$
- T1: mov R1, (counter) // counter = $1!$
- T1 stores one into counter
- Value of counter should have been two
- What if "counter++" is compiled into a single instruction, e.g., - "inc (counter)" ?

- T1: mov (counter), $R1 / R1 = 0$ $Ti: Add 1, R1$
- $\{switch-out, R1=1\text{ saved in }PCB\}$
- T2: mov (counter), R1 $//$ R₁ = \circ
- $T2: Add 1, R1$ // $R1 = 1$
- T2 mov R1, (counter) // counter = 1_{-}
- $\{switch-out, T1 scheduled, R1 = 1\}$
- T1: mov R1, (counter) // counter = $1!$
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- Value of counter should have been two
- What if "counter++" is compiled into a single instruction, e.g.,
	- "inc (counter)"?
	- Does not solve the issue on multi-processor systems!

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- If this function is executed by two threads, what will be the value of counter when two threads complete?

- Non-deterministic output
- Why?

Accessing shared variable in a concurrent manner results in incorrect output

Definitions

- Atomic operation: An operation is atomic if it is *uninterruptible* and indivisible
- Critical section: A section of code accessing one or more shared resource(s), mostly shared memory location(s)
- Mutual exclusion: Technique to allow exactly one execution entity to execute the critical section
- Lock: A mechanism used to orchestrate entry into critical section
- Race condition: Occurs when multiple threads are allowed to enter the critical section

Threads sharing the address space

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- μ - Everything seems to be fine, what is the issue?
- Sharp data is convenient to design parallel constructions of the share convenient of α - Example parallel computer computation models and computation models and computation models are considered and computation $\frac{1}{2}$ - Correctness of program impacted because of concurrent access to the shared data causes race condition
- \sim Data parallel processing: Data parallel processing: Data is partitioned in the sets and \sim - How does OS fit into this discussion?
	- assigned to different threads
	- Task parallel processing: Each thread performs a different computation on the same data

Critical sections in OS

- OS maintains shared information which can be accessed from different OS mode execution (e.g., system call handlers, interrupt handlers etc.)
- Example (1): Same page table entry being updated concurrently because of swapping (triggered because of low memory) and change of protection flags (because of mprotect() system call)
- Example (2): The queue of network packets being updated concurrently to deliver the packets to a process and receive incoming packets from the network device

Strategy to handle race conditions in OS

Threads sharing the address space

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- Everything seems to be fine, what is the issue?
- Correctness of program impacted because of concurrent access to the and data is convenient to design parallel computation of the state of the computation of
- How does OS fit into this discussion?
- Concurrency issues in OS is challenging as finding the race condition itself **is non-trivial** and the different threads

- Task parallel processing: Each thread performs a different computations and performs a different computation
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on the same data

Locking in pthread: pthread mutex

}

```
pthread mutex t lock; // Initialized using pthread mutex init
static int counter = o;
void *thfunc(void *)
{
 int ctr = 0;
 for(ctr=0; ctr<100000; ++ctr){
   pthread_mutex_lock(&lock); // One thread acquires lock, others wait 
   counter++; // Critical section
   pthread_mutex_unlock(&lock); // Release the lock
 }
```
Design issues of locks

pthread mutex t lock; // Initialized using pthread mutex init static int counter $= 0$;

- Efficiency of lock and unlock operations
- Lock acquisition delay vs. wasted CPU cycles
- $\sum_{i=1}^{n}$ int che est for the toching senemy - Fairness of the locking scheme

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$Lock$ ADT lock_t $*$ L1, L2;

 $lock_t * L;$

lock(L) { // Return \Rightarrow Lock acquired } unlock(L) { // Return \Rightarrow Lock released }

…. $lock(L1)$ Critical Section $unlock(L1)$ …. $lock(L2)$ Critical Section $unlock(L2)$ …. $Lock(L1)$ Critical Section $unlock(L2)$

Lock ADT: Efficiency

```
lock_t * L;lock(L)
{
 // Return \Rightarrow Lock acquired
}
unlock(L)
{
 // Return \Rightarrow Lock released
}
```
- Efficiency of lock/unlock operations directly influence performance
- Implementation choices?

Lock ADT: Efficiency

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 $lock(L)$

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{
 // Return \Rightarrow Lock acquired
}
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unlock(L)

}

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{
 // Return \Rightarrow Lock released
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- Efficiency of lock/unlock operations directly influence performance
- Implementation choices?
- Hardware assisted implementations
	- Use hardware synchronization primitives like atomic operations

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- Efficiency of lock/unlock operations directly influence performance
- Implementation choices?
- Hardware assisted implementations
	- Use hardware synchronization primitives like atomic operations
- Software locks are implemented without assuming any hardware support
	- Not used in practice because of high overheads

Design issues of locks

pthread mutex t lock; // Initialized using pthread mutex init static int counter $= 0$;

- Efficiency of lock and unlock operations
- Hardware-assisted lock implementations are used for efficiency
- $i = \frac{1}{2}$ ϵ for acquisition actu ϵ , ϵ - Lock acquisition delay vs. wasted CPU cycles
- p and p of the tocking scheme accuracy; p or p or p or p or p or p - Fairness of the locking scheme

}

}

 counter++; // Critical section pthread_mutex_unlock(&lock); // Release the lock

Lock: busy-wait (spinlock) vs. Waiting <u>ፐኒ</u> lock(L) //Acquired **T₂**

Critical section

unlock(L)

lock(L) //Lock is busy. Reschedule or Spin?

Critical section unlock(L)

Lock: busy-wait (spinlock) vs. Waiting <u>T1</u> lock(L) //Acquired Critical section $\mathbf{T2}$ lock(L) //Lock is busy. Reschedule or Spin?

 unlock(L) Critical section unlock(L)

- $\frac{1}{2}$ - With busy waiting, context switch overheads saved, wasted CPU cycles due to spinning
- Busy waiting is prefered when critical section is small and the context executing the critical section is not rescheduled (e.g., due to I/O wait)

Design issues of locks

pthread mutex t lock; // Initialized using pthread mutex init static int counter $= 0$;

- Efficiency of lock and unlock operations
- Hardware-assisted lock implementations are used for efficiency
- $i = \frac{1}{2}$ $\frac{1}{2}$ for acquisition actu $\frac{1}{2}$ is the set - Lock acquisition delay vs. wasted CPU cycles
- \sim 030 waiting to the and spiritually depending on the requirement - Use waiting locks and spinlocks depending on the requirement

pthread_mutex_unlock(&lock); // Release the lock (

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Fairness

- Given N threads contending for the lock, number of unsuccessful attempts for lock acquisition for all contending threads should be same

Fairness

- Given N threads contending for the lock, number of unsuccessful attempts for lock acquisition for all contending threads should be same
- Bounded wait property
	- Given N threads contending for the lock, there should be an upper bound on the number of attempts made by a given context to acquire the lock

Design issues of locks

pthread mutex t lock; // Initialized using pthread mutex init

- $\frac{1}{\sqrt{2}}$ $\sum_{i=1}^{n}$ - Efficiency of lock and unlock operations
- Hardware-assisted lock implementations are used for efficiency
- LOCK dCQU - Lock acquisition delay vs. wasted CPU cycles
- Use waiting locks and spinlocks depending on the requirement
- pthread active in the locking scheme accurate lock in the lock of the lock of the lock of the lock of the lock

}

}

- Contending threads should not starve for the lock indefinitely

pthread_mutex_unlock(&lock); // Release the lock