**Title:** VLSI Architectures for Training Deep Neural Networks and Homomorphic Encryption

**Speaker:** Professor Keshab K Parhi (University of Minnesota, Minneapolis)

**Date and Time:** 1st December 2022 (Thursday), 4 PM

**Venue:** Room 101, H R Kadim Diwan Building (KD 101), CSE Department

**Abstract:**

Machine learning and data analytics continue to expand the fourth industrial revolution and affect many aspects of our lives. The talk will explore hardware accelerator architectures for deep neural networks (DNNs). I will present a brief review of history of neural networks. I will then talk about reducing latency and memory access in VLSI accelerator architectures for training DNNs by gradient interleaving using systolic arrays. Then I will present our recent work on LayerPipe, an approach for training deep neural networks that leads to simultaneous intra-layer and inter-layer pipelining. This approach can increase processor utilization efficiency and increase speed of training without increasing communication costs. Finally, I will describe ongoing work on accelerators for computing in the encrypted domain, based on time-domain and frequency-domain approaches.

**Speaker Bio:**

Keshab K. Parhi received the B.Tech. degree from the Indian Institute of Technology (IIT), Kharagpur, in 1982, the M.S.E.E. degree from the University of Pennsylvania, Philadelphia, in 1984, and the Ph.D. degree from the University of California, Berkeley, in 1988. He has been with the University of Minnesota, Minneapolis, since 1988, where he is currently Erwin A. Kelen Chair in Electrical Engineering and Distinguished McKnight University Professor in the Department of Electrical and Computer Engineering. He has published 700 papers, is the inventor of 34 patents, and has authored the textbook VLSI Digital Signal Processing Systems (John Wiley & Sons, 1999). His current research addresses VLSI architecture design of machine learning systems, hardware security, data-driven neuroscience and DNA computing. Dr. Parhi is the recipient of numerous awards including the 2003 IEEE Kiyo Tomiyasu Technical Field Award, the 2017 Mac Van Valkenburg award and the 2012 Charles A. Desoer Technical Achievement award from the IEEE Circuits and Systems Society, and the 2004 F. E. Terman award from the American Society of Engineering Education. He received the 2013 Distinguished Alumnus award from IIT Kharagpur. He has served as the Editor-in-Chief of the IEEE Trans. Circuits and Systems, Part-I during 2004 and 2005. He is a Fellow of IEEE, ACM, AIMBE, AAAS and the National Academy of Inventors.