**Title:** Semantics-directed Shared Memory

**Abstract:** The shared memory consistency model is the critical hardware-software interface in multiprocessors that specifies what value a read must return. However, this seemingly simple interface has been facing a number of notorious challenges including: (1) unclear specification; (2) implementation riddled with bugs; (3) tension between programmability and efficiency. In this talk, I will first overview the work we've been doing for the past decade in addressing these challenges.

Midway into our research, we realized a key insight underpinning our work. Hardware design for shared memory should not be guided by ad-hoc informal specifications. Instead, we advocate for implementations to be derived from the specification through a series of refinements. This not only leads to designs that are correct but also (somewhat surprisingly) to designs that are efficient.

Based on this realization, I will outline our vision for synthesizing efficient and correct-by-construction shared memory systems. As a first step towards this goal, I will talk about ProtoGen, our tool for synthesizing highly-concurrent non-blocking coherence protocols given only their atomic (stable state) specifications.

**Bio:** Vijay Nagarajan is a Reader (Associate Professor) at the University of Edinburgh. His research interests span computer architecture, compilers and computer systems with a focus on consistency models and coherence protocols. Vijay is a recipient of an Intel Early Career Faculty Award, a best-paper award at PACT, an IEEE Top-Pick Honourable mention and a number of HiPEAC paper awards.